REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on May 30, 2003, and the references cited therewith.

Claims 2, 5, 6, 11, 35, and 36 are amended. No claims are currently cancelled or added. As a result, claims 2, 3, 5-8, 11, 12, and 30-37 are now pending in this application.

Claim Objections

Claims 35 and 36 are objected to due to informalities. Applicant has corrected the informalities pointed out by the Examiner. Accordingly, Applicant respectfully requests that the Examiner withdraw the objection to claims 35 and 36.

§102 Rejection of the Claims

Claim 2 was rejected under 35 USC § 102(e) as being anticipated by Devoe et al. (U.S. 6,366,443). Applicant has amended claim 2 in order to more clearly distinguish it from that which is disclosed by Devoe et al. In light of the amendment to claim 2 and the remarks, below, Applicant respectfully traverses the rejection.

Devoe et al. disclose a ceramic capacitor (1a-h, Figs. 1a-h), which includes interior metallization planes (1b10, 1b11, Fig. 1b) connected to areas of metallization or pads (1b2, 1b3, Fig. 1b) on exterior surfaces through vias (1b40, 1b41). (See Abstract and Figures 1a-h, 2a-c, 3b, 11).

Applicant's claim 2 includes at least the following limitations, which distinguish claim 2 from that which is disclosed in Devoe et al.:

Limitations of Claim 2	Devoe et al.
". . . a plurality of vias . . . , wherein the plurality of vias includes a first set of vias and a second set of vias, and the first set of vias couples the first plurality of conductive layers to a first plurality of connection sites on at least two surfaces of the capacitor, and the first set	Nowhere do Devoe et al. disclose a via that extends through, but is electrically isolated from any of the interior layers. Instead, as Figures 1a-h and 3c of Devoe et al. illustrate, vias are never shown to extend through an opening in any interior plane. Nor do Devoe et

of vias extends through openings in and is electrically isolated from the second plurality of conductive layers, and the second set of vias couples the second plurality of conductive layers to a second plurality of connection sites on the at least two surfaces, and the second set of vias extends through openings in and is electrically isolated from the first plurality of conductive layers . . .."	al. show vias that couple a conductive layer to connection sites on at least two surfaces of the capacitor.

Support for the amendment to claim 2 can be found in the specification at page 3, lines 26-28, and in Figure 1A. Based on the above, Applicant believes that Devoe et al. do not disclose the limitations of Applicant's claim 2, and that claim 2 is in a condition for allowance. Accordingly, Applicant respectfully requests that the Examiner reconsider the rejection, and allow claim 2.

§103 Rejection of the Claims

Claims 5 and 32-33

Claims 5 and 32-33 were rejected under 35 USC § 103(a) as being unpatentable over Stone (U.S. 5,530,288) in view of Farooq et al. (U.S. 6,072,690). Applicant has amended claim 5 in order to more clearly distinguish it from that which is disclosed by Stone in combination with Farooq et al. In light of the amendment to claim 5 and the remarks, below, Applicant respectfully traverses the rejection.

Stone discloses an interposer (100, Fig. 1), which can have a passive electronic component (17, Fig. 1) attached to an electrically conductive plane (21, Fig. 1) within the interposer. Figure 1 shows through holes (5) in the interposer (100). Applicant does not agree with the statement that Stone discloses a capacitor connected to connection sites with a plurality of through holes. The through holes of Stone are through holes in the interposer (100), and not through holes within the passive component (17) itself. Nowhere does Stone discuss the internal structure of a capacitor. Accordingly, Applicant believes that Stone is an irrelevant reference,

and is not properly combinable with Farooq et al. or any other reference that pertains to a capacitor.

Farooq et al. disclose a ceramic capacitor (60, Fig. 3A) having vias (64, 66) that are formed by filling holes with a metal paste. (See col. 6, lines 30-33).

Applicant's claims 5, 30, and 32 include at least the following limitations, which distinguish claims 5, 30, and 32 from that which is disclosed in Stone, Farooq et al., or their combination:

Limitations of Claims 5, 32, 33	Stone and Farooq et al.
". . . a plurality of vias coupling the at least four conductive layers to a plurality of connection sites on at least two surfaces of the capacitor, wherein the plurality of vias includes a first set of vias and a second set of vias, and the first set of vias couples the first plurality of conductive layers to a first plurality of connection sites on the at least two surfaces of the capacitor, and the first set of vias extends through openings in and is electrically isolated from the second plurality of conductive layers, and the second set of vias couples the second plurality of conductive layers to a second plurality of connection sites on the at least two surfaces, and the second set of vias extends through openings in and is electrically isolated from the first plurality of conductive layers, and wherein the plurality of vias are plated through holes."	As Applicant discussed above, Stone pertains to an interposer structure, and not a capacitor structure. Therefore, the plated through holes of Stone are not obviously combinable or useful in a capacitor structure. Further, nowhere does Farooq et al. disclose a capacitor having vias that are plated through holes. Instead, the vias of Farooq et al. are filled with a metal paste.

Support for the amendment to claim 2 can be found in the specification at page 3, lines 26-28, and in Figure 1A. Based on the above, Applicant believes that the combination of Stone

and Farooq et al. neither discloses, suggests nor motivates the limitations of Applicant's claims 5, 32, or 33, and that claims 5, 32, and 33 are in a condition for allowance. Accordingly, Applicant respectfully requests that the Examiner reconsider the rejection, and allow claims 5, 32, and 33.

Claims 3 and 30-31

Claims 3 and 30-31 were rejected under USC § 103(a) as being unpatentable over Devoe et al.. Applicant discussed the Devoe et al. reference above, in conjunction with the remarks concerning the rejection of claim 2 under 35 USC § 102(e). Each of claims 3 and 30-31 depend from claim 2, which Applicant believes to be in a condition for allowance. Accordingly, Applicant believes that claims 3 and 30-31 also are in a condition for allowance, and respectfully requests that the Examiner reconsider and withdraw the rejection of claims 3 and 30-31.

Further, Applicant respectfully traverses the single reference rejection under 35 U.S.C. § 103 since not all of the recited elements of the claims are found in Devoe et al.. Since all the elements of the claims are not found in the reference, Applicant assumes that the Examiner is taking Official Notice of the missing elements. Applicant respectfully objects to the taking of Official Notice with a single reference obviousness rejection and, pursuant to M.P.E.P. § 706.02(a), Applicant respectfully traverses the assertion of Official Notice and requests that the Examiner cite references in support of this position.

Claims 6-8

Claims 6-8 were rejected under USC § 103(a) as being unpatentable over Farooq et al. in view of Mori (U.S. 5,942,063). Applicant has amended claim 6 in order to more clearly distinguish it from that which is disclosed by Farooq et al. in combination with Mori. In light of the amendment to claim 6 and the remarks, below, Applicant respectfully traverses the rejection.

Farooq et al. disclose a ceramic capacitor (60, Fig. 3A) having vias (64, 66) that are formed by filling holes with a metal paste. (See col. 6, lines 30-33).

Mori discloses a method of preparing a multilayer ceramic component. (See Abstract).

Applicant's claims 6-8 include at least the following limitations, which distinguish claims 6-8 from that which is disclosed in Farooq et al., Mori or their combination:

Limitations of Claims 6-8	Farooq et al. and Mori
". . . a pair of dielectric sheets formed from barium titanate . . ."	Both Farooq et al. and Mori pertain to capacitors having ceramic dielectric layers. Nowhere do Farooq et al., Mori or their combination disclose, suggest or motivate using barium titanate as a dielectric layer.

Support for the amendment to claim 6 can be found in the specification at page 5, lines 10-11. Based on the above, Applicant believes that the combination of Farooq et al. and Mori neither discloses, suggests nor motivates the limitations of Applicant's claims 6-8, and that claims 6-8 are in a condition for allowance. Accordingly, Applicant respectfully requests that the Examiner reconsider the rejection, and allow claims 6-8.

Claims 11-12 and 36

Claims 11-12 and 36 were rejected under USC § 103(a) as being unpatentable over Farooq et al. in view of Naito et al. (U.S. 6,034,864). Applicant has amended claim 11 in order to more clearly distinguish it from that which is disclosed by Farooq et al. in combination with Naito et al. In light of the amendment to claim 11 and the remarks, below, Applicant respectfully traverses the rejection.

Farooq et al. disclose a ceramic capacitor (60, Fig. 3A) having vias (64, 66) that are formed by filling holes with a metal paste. (See col. 6, lines 30-33).

Naito et al. disclose a multilayer ceramic capacitor (31, Fig. 1) having internal electrodes (33, 34) , and connection portions (40, 41), which couple to external electrodes (38, 39). (See col. 5, lines 6-34, and Fig. 2A). A specific example is given of a capacitor with forty (40) internal electrodes and twenty-five (25) connection portions. (See col. 6, lines 56-62).

Applicant's claims 11-12 and 36 include at least the following limitations, which distinguish claims 11-12 and 36 from that which is disclosed in Farooq et al., Naito et al. or their combination:

Limitations of Claims 11-12 and 36	Farooq et al. and Naito et al.
". . . a multilayered capacitor having a pair of	Both Farooq et al. and Naito et al. pertain to

substantially rigid outer surfaces formed from barium titanate . . ."	capacitors having ceramic dielectric layers. Nowhere do Farooq et al., Naito et al. or their combination disclose, suggest or motivate using barium titanate as an outer surface.
" . . . the multilayered capacitor includes a number of parallel conductive layers . . . and wherein the number of conductive layers is greater than about 50. . ."	Naito et al. only gives an example of a capacitor with forty (40) electrodes. Applicant requests that the Examiner provide a specific reference indicating that an analogous capacitor contains greater than about 50 conductive layers.
" . . . wherein the number of pads is greater than about 4000."	Naito et al. only gives an example of a capacitor with twenty-five (25) connection portions. Applicant requests that the Examiner provide a specific reference indicating that an analogous capacitor contains greater than about 4000 pads.

Support for the amendment to claim 11 can be found in the specification at page 5, lines 10-11. Based on the above, Applicant believes that the combination of Farooq et al. and Naito et al. neither discloses, suggests nor motivates the limitations of Applicant's claims 11-12 and 36, and that claims 11-12 and 36 are in a condition for allowance. Accordingly, Applicant respectfully requests that the Examiner reconsider the rejection, and allow claims 11-12 and 36.

Claims 34-35 and 37

Claims 34-35 and 37 were rejected under USC § 103(a) as being unpatentable over Farooq et al. and Naito et al. in view of Mori. Applicant discussed the Farooq et al., Naito et al., and Mori references above. Each of claims 34-35 and 37 depend from claim 11, which Applicant believes to be in a condition for allowance. Accordingly, Applicant believes that claims 34-35 and 37 also are in a condition for allowance, and respectfully requests that the Examiner reconsider and withdraw the rejection of claims 34-35 and 37.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, Sherry Schumm ((480) 657-3766) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LARRY E. MOSLEY

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation
P.O. Box 2938
Minneapolis, Minnesota 55402
(612) 371-2109

Date August 29, 2003

By _____
Danny J. Padys
Reg. No. 35,635

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 29 day of August, 2003.

KACIA LEE
Name

Kacia Lee
Signature